Upset Characterization

of the

PowerPC405 Hard-Core Processor Embedded in Virtex-II Pro Field Programmable Gate Arrays

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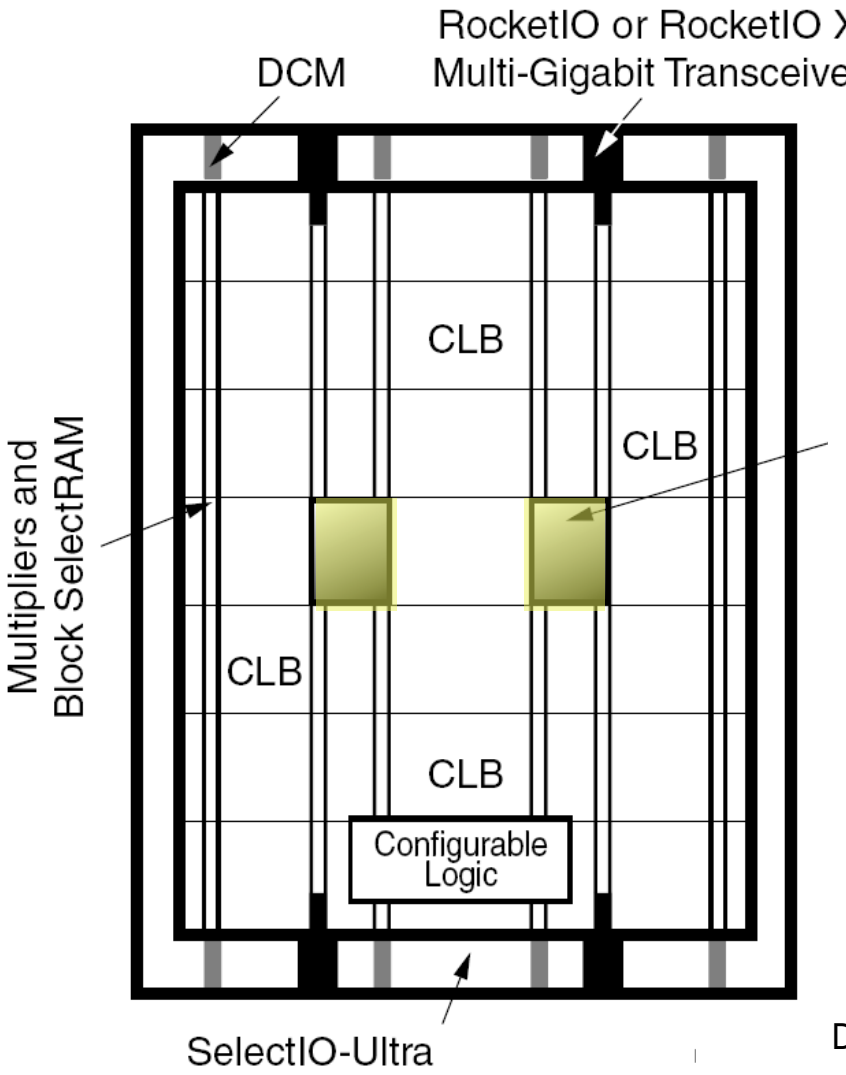
Abstract

Shown in this presentation are recent results for the upset susceptibility of the various types of memory elements in the embedded PowerPC405 in the Xilinx V2P40 FPGA. For critical flight designs where configuration upsets are mitigated effectively through appropriate design triplication and configuration scrubbing, these upsets of processor elements can dominate the system error rate. Data from irradiations with both protons and heavy ions are given and compared using available models.

Device Under Test

The 2VP40 device from the Xilinx Virtex-IIPro family includes two 300 MHz-capable IBM PPC405 processors; this device was irradiated for this work. The device is fabbed in a 130 nm CMOS process with commercial devices on bulk CMOS or a thick epitaxial layer and the Mil/Aero devices on thin-epi CMOS. In addition to the pair of PPC cores and almost 20,000 configurable logic blocks, this FPGA has the following features available for inclusion in a design: 3.5Mb of user RAM, 192 hardware multipliers, 804 I/O's with 12 so-called RocketIO Transceivers capable of speeds up to 3 Gb/s, and 8 digital clock manager blocks. The PPC405 is a 32-bit, integer-only microcontroller cousin to the PPC750 with which it shares its instruction set.

Device Under Test - Floor Plan



Processor Block

DCM = Digital Clock Manager

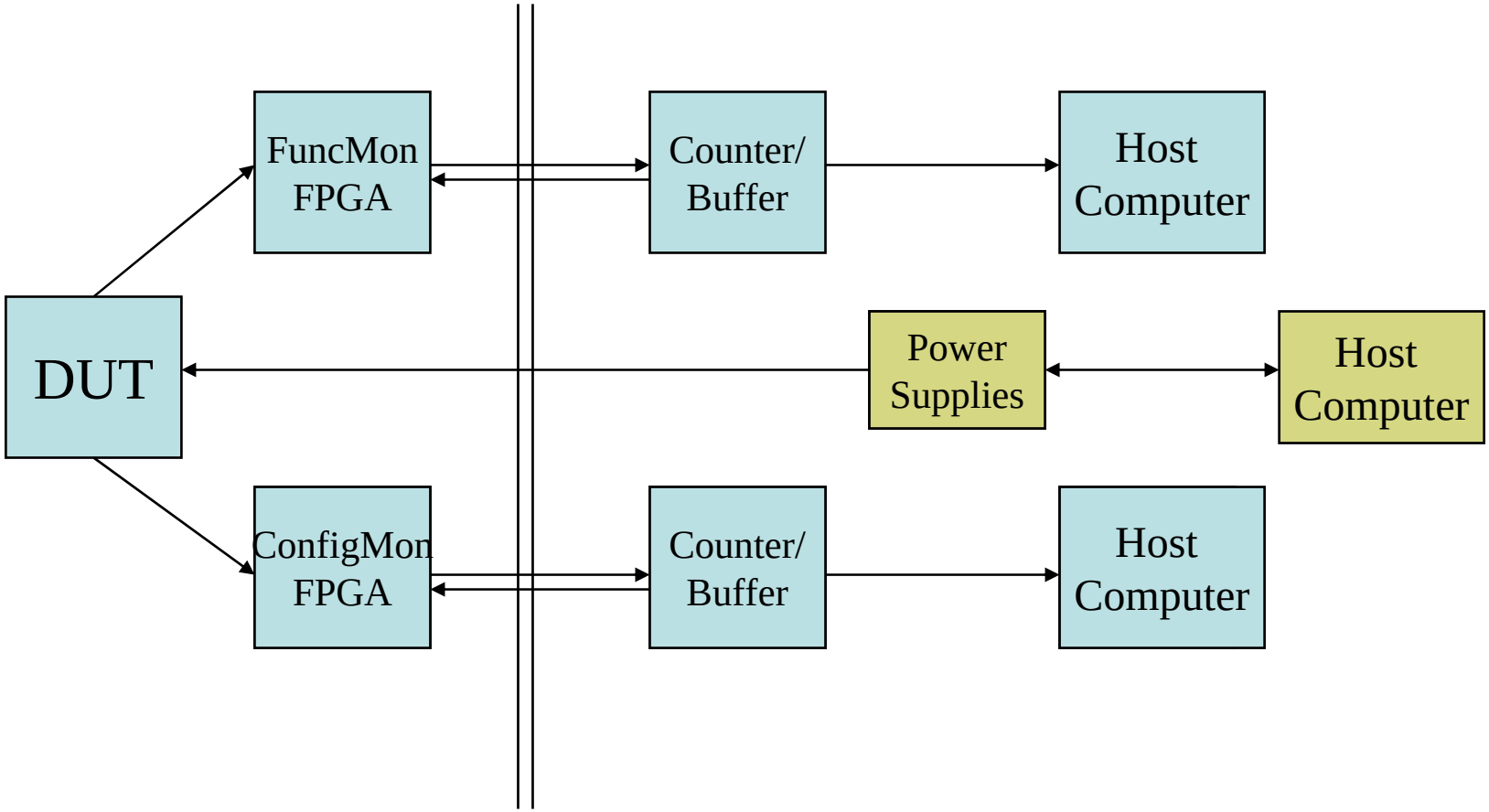
CLB = Configuration Logic Block

Device Under Test - Storage Elements

Name	Description	# of bits	Percent
CLB	**Configuration SRAM**	**10,462,828**	**71.443%**
BRAM *	**Design-level SRAM**	**3,538,944**	**24.165%**
FF	**Design-level Flip-Flops**	**38,784**	**0.265%**
-- Total *OUTSIDE* Processor Cores --		**14,040,556**	**95.873%**
I Cache	**Instruction Cache**	**262,144**	**1.790%**
D Cache	**Data Cache**	**262,144**	**1.790%**
GPRs	**General Purpose Registers**	**2,048**	**0.014%**
SPRs	**Special Purpose Registers**	**3,456**	**0.024%**
-- Total *INSIDE* Processor Cores ** **--**		**529,792**	**3.618%**
gasket	**PPC-to-CLB interface**	**74,592**	**0.509%**
	Grand Total	**14,644,940**	**100%**

Note that the processor inventory here is incomplete; there are an unknown number of internal control and state machine bits.

Test Setup


FuncMon FPGA
Counter/ Buffer
Host Computer
DUT
Power Supplies
Host Computer
ConfigMon FPGA
Counter/ Buffer
Host Computer

Test Setup

DUT runs code from triplicated internal block RAM and communicates through triplicated I/O's and (minimal) triplicated gate array "fabric"

Four separate instrumentation legs – each with logging

- Configuration upsets are monitored and scrubbed by ConfigMon
- Upsets in registers and translation look-aside buffers (TLBs) are reported via the functional monitor leg – FuncMon
- Post-beam cache dumps through processor debug port using an Agilent probe (leg not shown)
- Power and temperature monitoring leg

Test Method

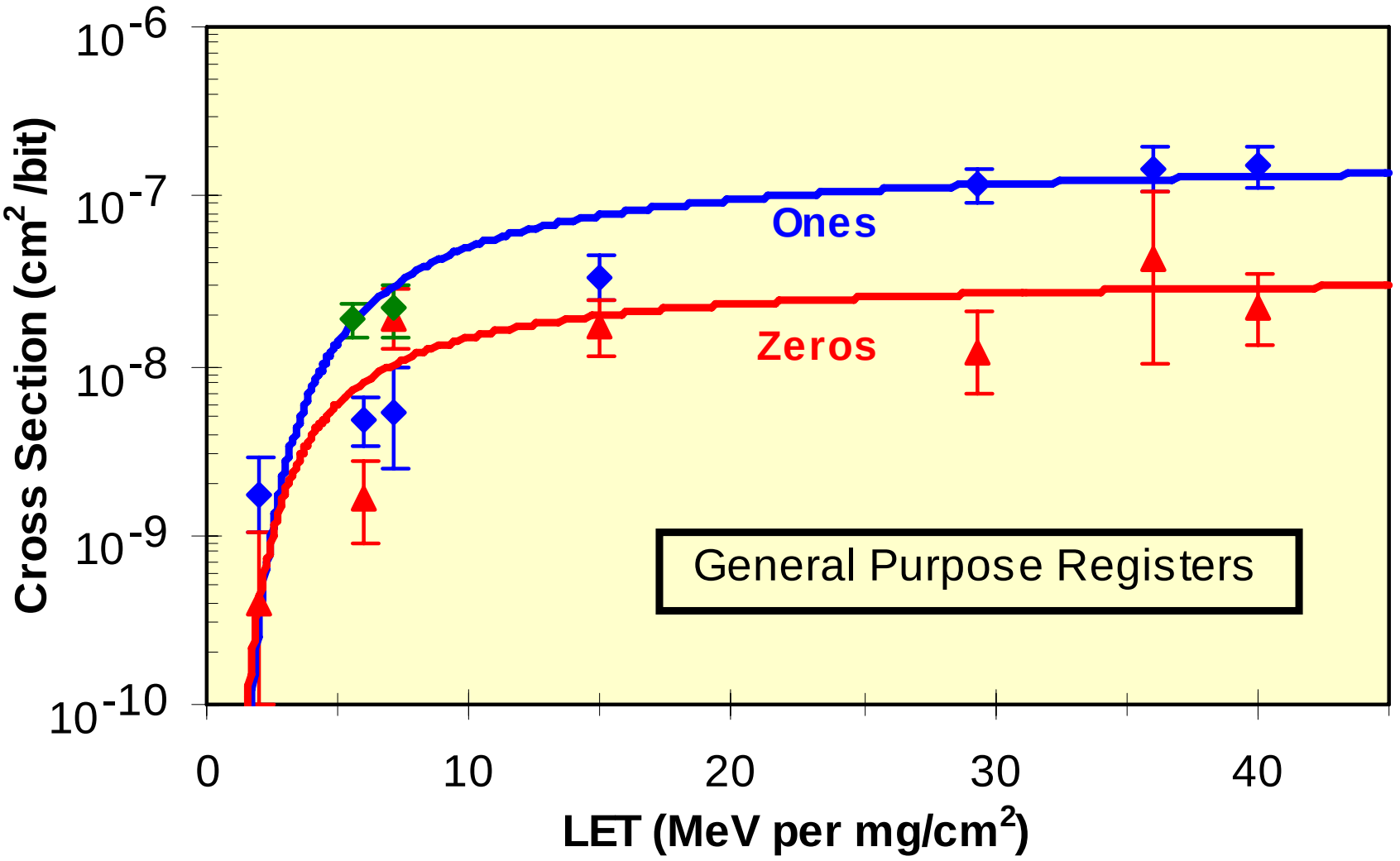
Pseudo-static

- Clocked, but with minimal processor activity
- aka “do little” - see [SwF01]

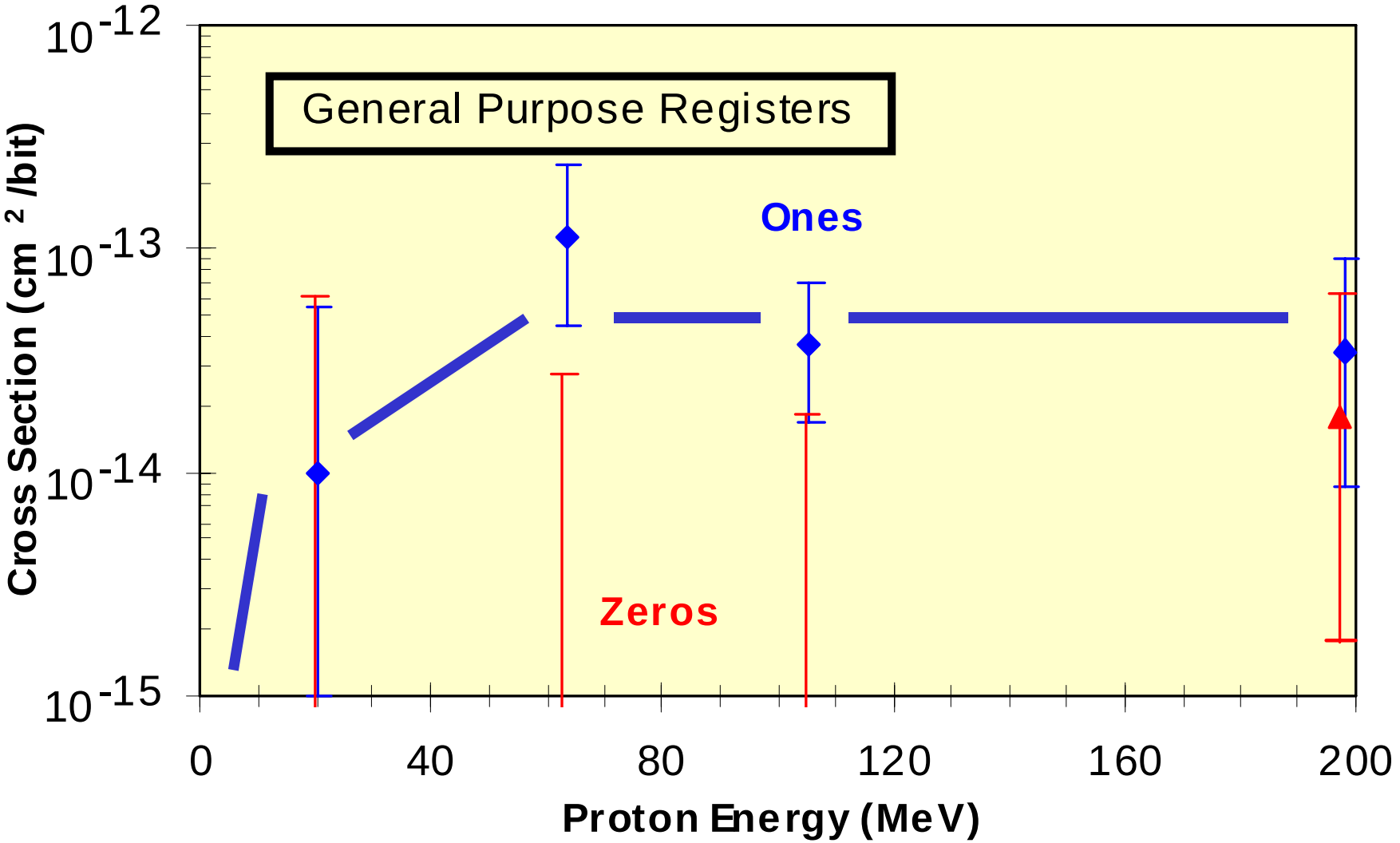
Dynamic

- Running counter or Dhrystone benchmark [Glo05]
- aka “application” testing

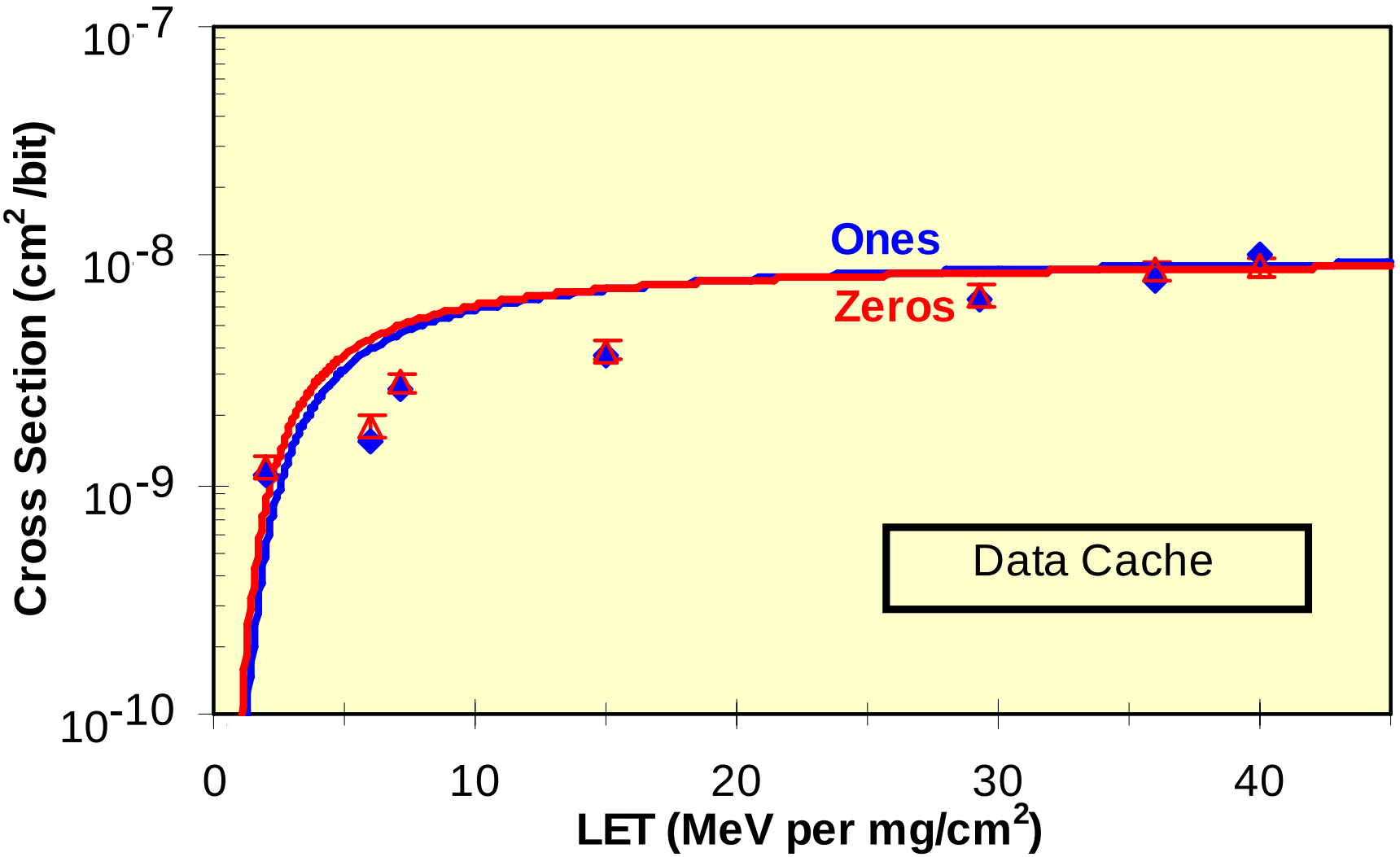
Static Test Results - Heavy Ions



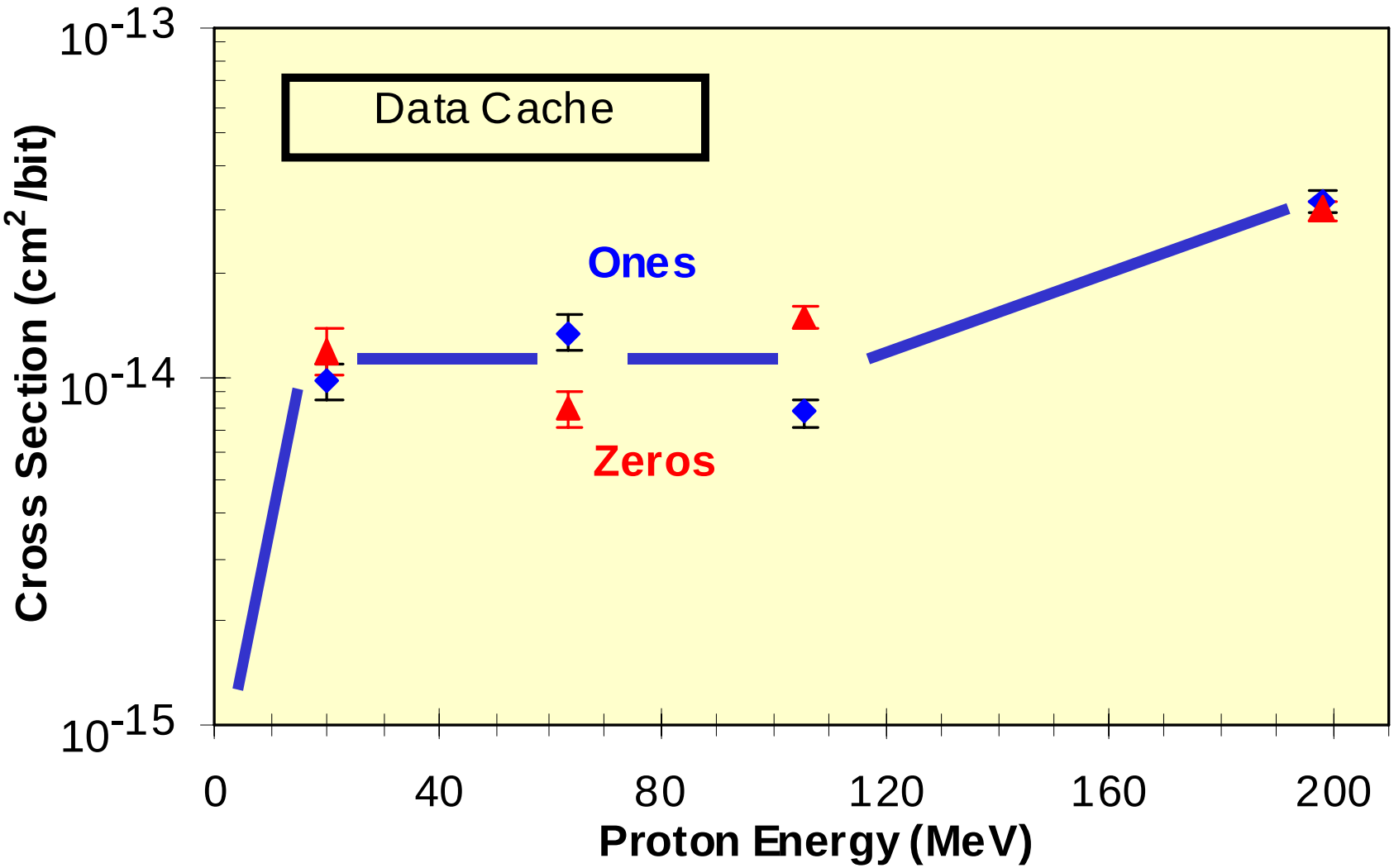
Static Test Results - Protons



Static Test Results - Heavy Ions



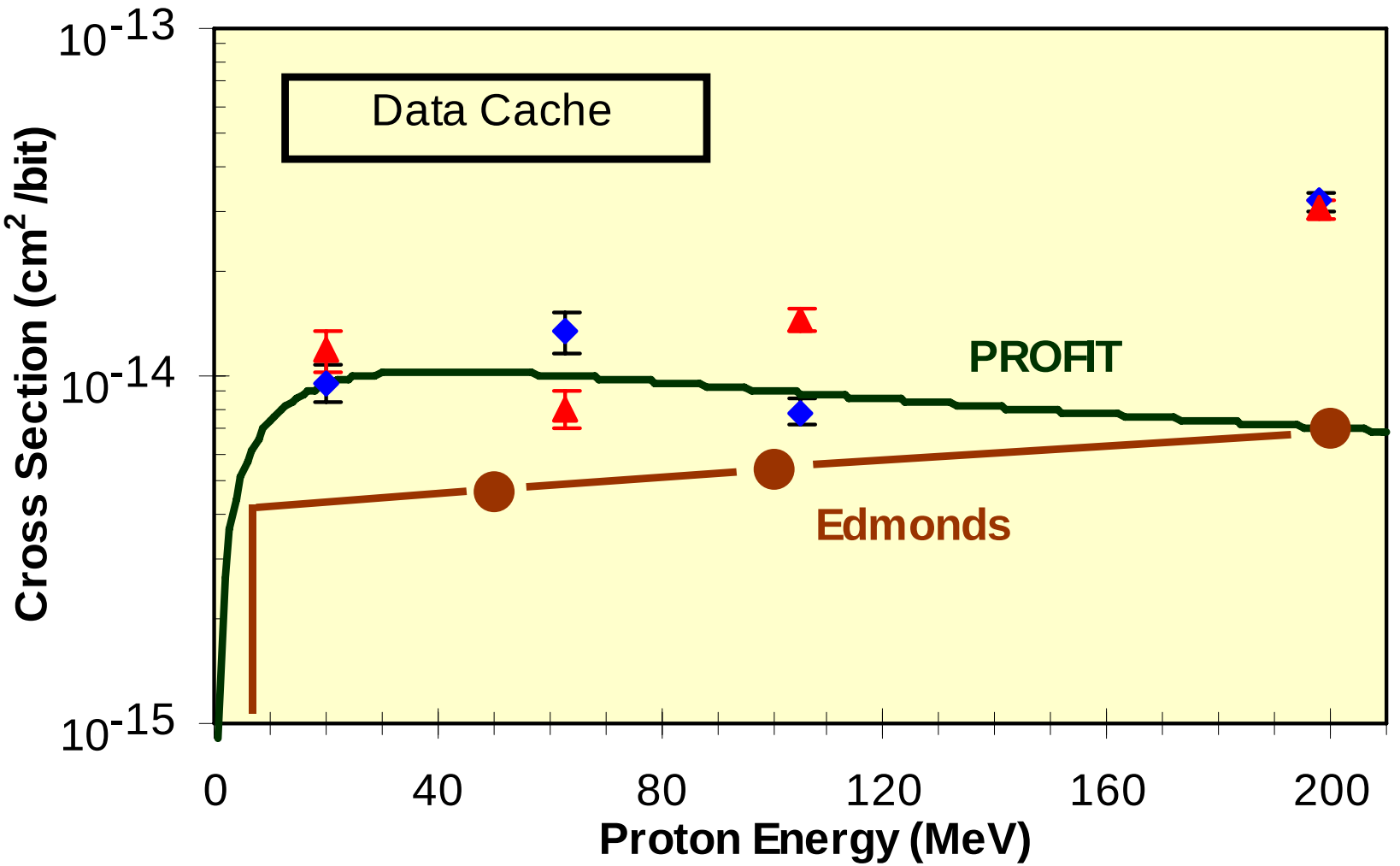
Static Test Results - Protons



Dynamic Test Results

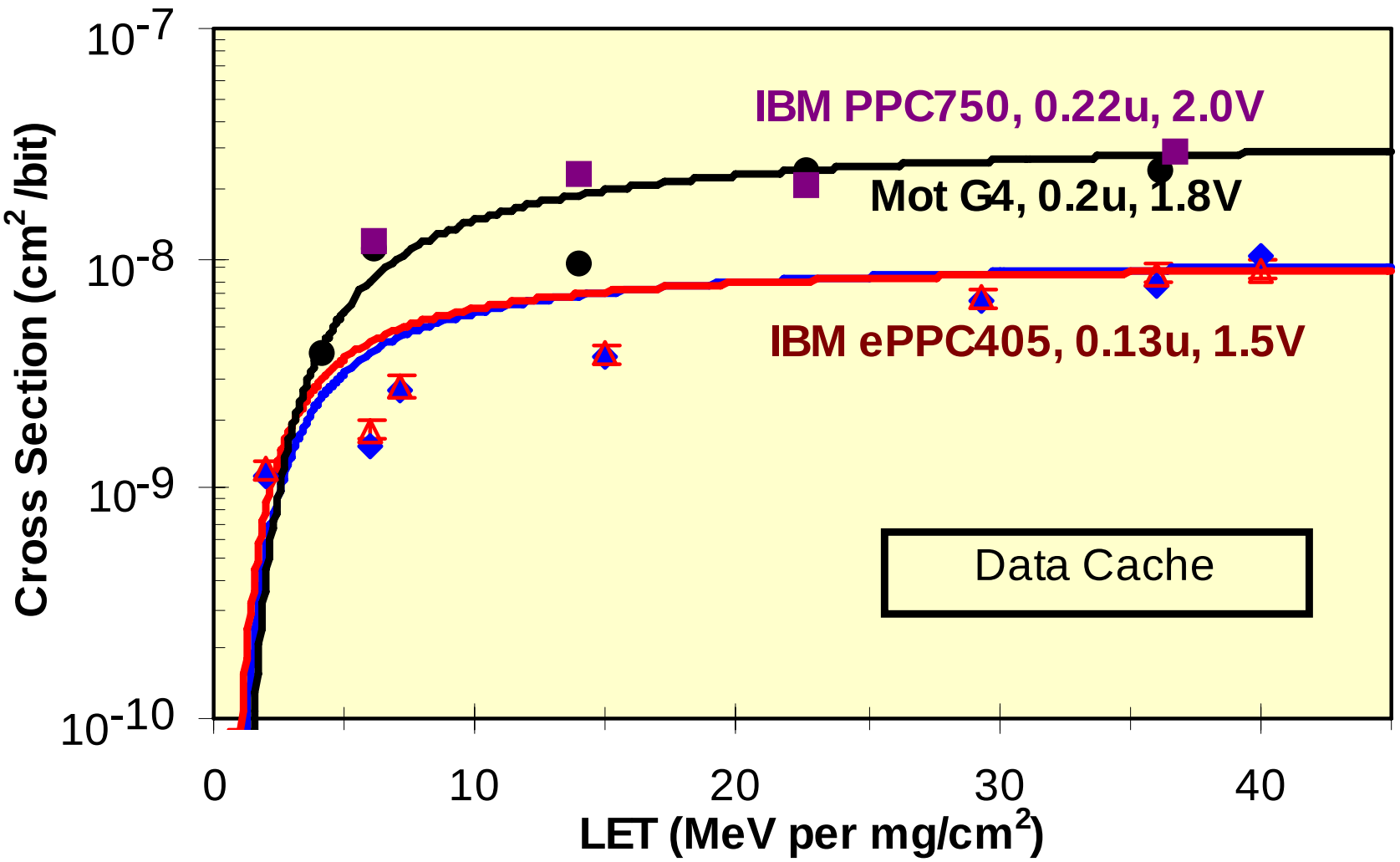
- Program “hangs” (from hitting an important special purpose register, for example) typically ended irradiation runs.
- Consistent with earlier results [Bez97], dynamic testing yields lower error cross sections than static testing by as much as two orders of magnitude (not all bits are important all the time in running application software).
- At core frequencies up to 300 MHz, there is little dependence on clock frequency.

Model Comparison Example



PROFIT model with two fitting parameters from [Cla96] and Edmonds model with no fitting parameters from [Edm00]

Scaling Comparison



Upset Rates in the GCR Background

Approximate rates of upset in the solar minimum Galactic Cosmic Ray (GCR) background are:

2 configuration upsets per day

2 cache upsets per month

2 register upsets per year

2 SEFIs per century

- Appropriate design triplication combined with active scrubbing eliminates system errors from configuration upsets.
- As a result, cache and processor upsets will be the dominant source of system errors.

Conclusions

- Static test results are conservative

  Bit cross sections times the total number of bits yields too high a result because not all bits are important all the time.

- Dynamic test results are in frequency independent regime, at present

- Both PROFIT and Edmonds models under-predict proton results

  Using heavy ion data to predict proton results gave a result about four or five times lower than the actual data.

- Scaling feature size by 40% and core voltage by 20% lowered the high-LET cross section by about a factor of three but did not affect the LET threshold.

References

[Bez97] F. Bezerra et al., “Commercial processor single event tests,” *RADECS Conf. Data Workshop Record*, 1997, pp. 41–46.

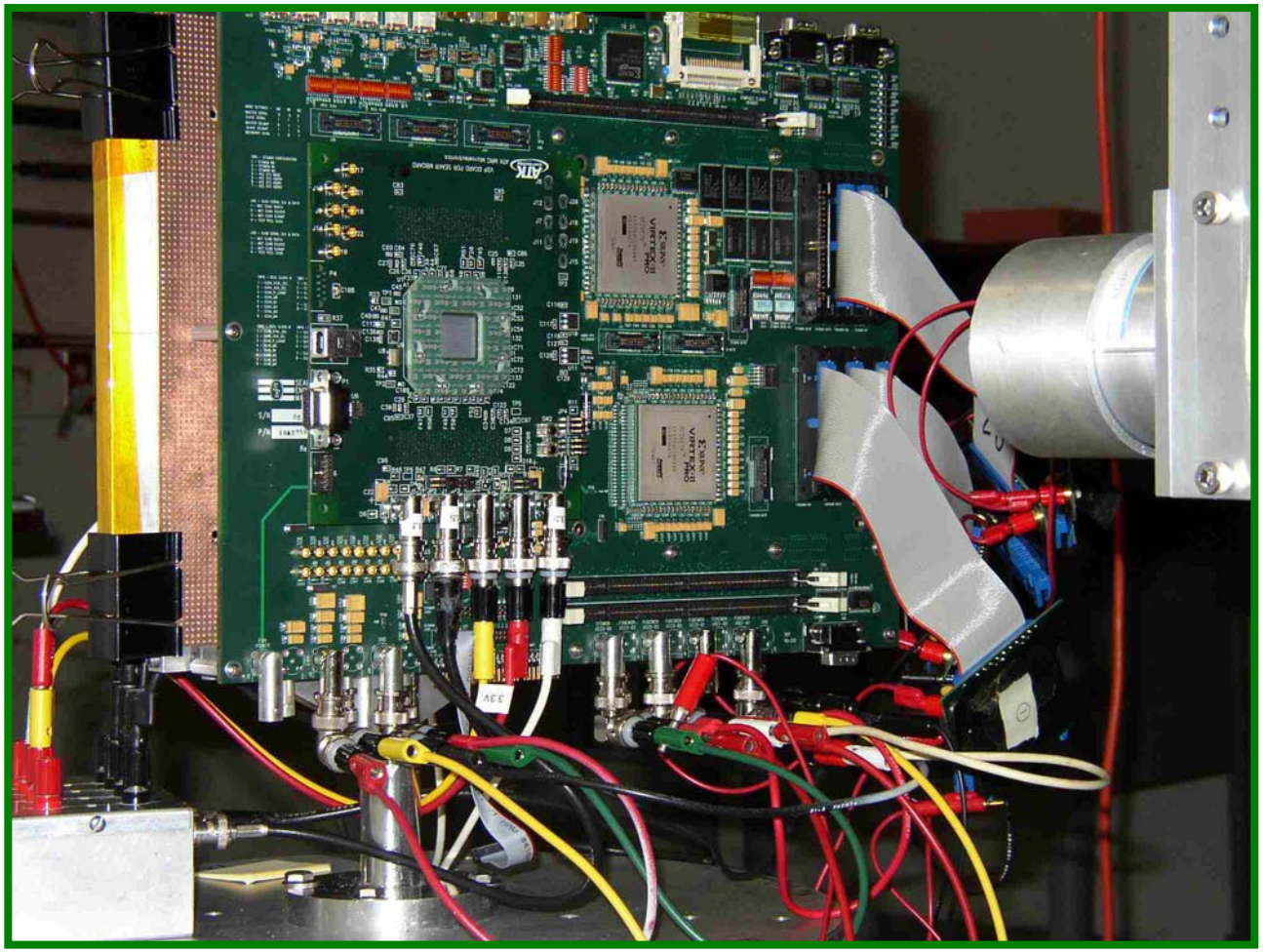
[Cla96] P. Calvel et al, "An empirical model for predicting proton induced upset," IEEE Trans. Nucl. Sci., vol. NS-43, no. 6, pp. 2827-2832, 1996.

[Edm00] Larry D. Edmonds, "Proton SEU cross sections derived from heavy-ion test data," IEEE Trans. Nucl. Sci., vol 47, no. 5, 2000.

[SwF01] G. Swift, F. Farmanesh, et al., “Single Event Upset in the PowerPC750 Processor,” *IEEE Trans. Nucl. Sci.*, vol. NS-47, no. 6, pp. 1822-1827, Dec. 2001.

[Glo05] P. Glover, “Running the Dhrystone 2.1 Benchmark on a Virtex-II Pro PowerPC Processor, Xilinx Application Note 507, July 2005, http://www.xilinx.com/bvdocs/appnotes/xapp507.pdf .

Test Setup



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